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EXAMINER	
TECKLU, ISAAC TUKU	
ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,747	MOIR ET AL.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :01/31/06, 12/30/05, 12/20/05, 09/29/04, 06/17/04.

DETAILED ACTION

1. This action is responsive to the application filed on 07/16/2003.

2. Claims 1-59 have been examined.

Oath/Declaration

3. The office acknowledges receipt of a properly signed oath/declaration filed on 07/16/2006.

Specification

4. The disclosure is objected to because of the following informalities: The specification is devoid of terms such as "computer program product" and "computer-readable medium" as recited in claims 44-45, and 46-55, respectively. The specification is inconsistent with terms recited in claims 44-45, and 46-55. The specification should be written in "full, clear, concise, and exact terms". Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 46-55 recite "computer-readable medium" defined to include wireless or other communication medium (in claim 55). Thus, under the Interim Guidelines such media do not fall within one of the four statutory classes of 35 U.S.C. 101 (See Annex IV). Therefore, the above claims are non-statutory.

A computer-readable media is a tangible physical article or object, some form of matter, which a signal (infrared)/carrier wave is not. That the other two product classes, machine and composition of matter, require physical matter is evidence that a manufacture was also intended to require physical matter. A signal/carrier wave, a form of energy, does not fall within either of

the two definitions of manufacture. Thus, a signal/carrier wave does not fall within one of the four statutory classes of Sec. 101.

See Annex IV (c) Electro-Magnetic Signals, Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility (signed October 26, 2005) – OG Cite: 1300 OG 142. Online version can be retrieved at <http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm>

Under the principles of compact prosecution, claims 46-55 have been examined as the Examiner anticipates the claims will be amended to obviate these 35 USC 101 issues. For example, A computer-readable physical storage medium...-

Claims 47-55 are rejected for failing to cure the deficiencies of the above rejected non-statutory claim above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dice et al. (US 6,799,236 B1) in view of Newell et al. (US 5,918,248).

Per claim 1, Dice discloses a method of providing non-blocking multi-target transactions in a computer system (e.g. FIG. 2, 206 and FIG. 6 and related text), the method comprising:

defining plural transactionable locations (e.g. FIG. 3, 252, 253 and related text), wherein individual ones of the transactionable locations encode respective values and are owned by no more than one transaction at any given point in a multithreaded computation (col. 27: 1-15 "... predefined values into memory locations that can be modified ..."); for a particular multi-target transaction of the multithreaded computation, attempting to acquire ownership of each of the transactionable locations targeted thereby (col. 3:15-30 "... CAS instruction at the end ... attempts to successfully execute ... each time this instruction fail ..."), wherein the ownership acquiring rests ownership from another transaction, if any, that owns the targeted transactionable location (e.g. FIG. 5, SET INTERFERENCE SIGNAL TO INDICATE RESET VALUE 405 and related text); and

once ownership of each of the targeted transactionable locations has been acquired, attempting to commit the particular multi-target transaction using a single-target synchronization primitive to ensure that, at the commit (col. 21: 15-25 "... memory information committed such as writing the contents of registers out ...")

Dice does not explicitly discloses the particular multi-target transaction continues to own each of the targeted transactionable locations, wherein individual ones of the multi-target transactions do not contribute to progress of another. However, Newell discloses blocking or committing will occur when a task attempts to access a memory location which is owned by another task (e.g. FIG. 8 and 9). If the blocked task is allowed to continue, then a state transition back to ACTIVE (bubble 204) for that task occurs, and the blocking task undergoes a state transition from ACTIVE (bubble 204) to ROLLBACK (bubble 208) of FIG. 8 (col. 9:20-35). Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to combine Dice and Newell to continue the ownership locations by disallowing state transition for the blocked task in the ACTIVE state as once suggested by Newell col. 9:20-35).

Per claim 2, Dice discloses the method of claim 1, wherein the ownership wresting employs a single-target synchronization primitive to change status of the wrested from

transaction to be incompatible with a commit thereof (col. 21: 1-15 "... change during interruption ...").

Per claim 3, Dice discloses the method of claim 2, wherein, as a result of the status change, the wrested from transaction fails and retries (col. 3:15-30 "... CAS instruction at the end ... attempts to successfully execute ... each time this instruction fail ...").

Per claim 4, Dice discloses the method of claim 2, wherein the wrested from transaction is itself a multi-target transaction (col. 25: 30-45 "... one or more transactions ..." and e.g. FIG. 6, 419 and related text).

Per claim 5, Dice discloses the method of claim 1, further comprising: on failure of the commit attempt, reacquiring ownership of each targeted transactionable location and retrying (col. 3:15-30 "... CAS instruction at the end ... attempts to successfully execute ... each time this instruction fail ...").

Per claim 6, Dice discloses the method of claim 1, wherein no transaction may prevent another from wresting therefrom ownership of transactionable locations targeted by the active transaction (col. 6: 45-50 "... can not do so due to the lock ...").

Per claim 7, Dice discloses the method of claim 1, wherein the ownership acquiring employs a single-target synchronization primitive to update the ownership of the targeted transactionable location (col. 8: 1-15 "... update the current state ...").

Per claim 8, Dice discloses the method of claim 1, wherein each encoding of a transactionable location is atomically updateable using a single-target synchronization primitive (col. 13: 57-67 "... memory is encoded ...").

Per claim 9, Dice discloses the method of claim 1, wherein the individual transactionable location encodings further include an identification of the owning transaction's corresponding

value for the transactionable location (col. 16: 55-65 "... identification indicating an identity ...").

Per claim 10, Dice discloses the method of claim 1, further comprising: accessing values corresponding to individual ones of the transactionable locations using a wait-free load operation (col. 16: 55-67 "... information can include register values ...").

Per claim 11, Dice discloses the method of claim 1, wherein the transactionable locations directly encode the respective values (col. 16: 55-67 "... information can include register values ...").

Per claim 12, Dice discloses the method of claim 1, wherein the transactionable locations are indirectly referenced (col. 16: 55-67 "... information can include register values ...").

Per claim 13, Dice discloses the method of claim 1, wherein the transactionable locations are encoded in storage managed using a nonblocking memory management technique (col. 10: 10-20 "... technique lock-free ...").

Per claim 14, Dice discloses the method of claim 1, wherein the transactionable locations, if unowned, directly encode the respective values and otherwise encode a reference to the owning transaction (col. 6: 45-50 "... inability to obtain ownership ...").

Per claim 15, Dice discloses the method of claim 1, wherein the single-target synchronization primitive employs a Compare-And-Swap (CAS) operation (col. 3: 25-30 "... CAS...").

Per claim 16, Dice discloses the method of claim 1, wherein the single-target synchronization primitive employs Load-Linked (LL) and Store-Conditional (SC) operation pair (col. 3: 60-65 "LL... SC ...").

Per claim 17, Dice discloses the method of claim 1, wherein the single-target of the single-target synchronization primitive includes at least a value and a transaction identifier encoded integrally therewith (col. 16: 55-67 "... information can include register values ...").

Per claim 18, Dice discloses the method of claim 1, wherein the multi-target transaction has semantics of a multi-target compare and swap (NCAS) operation (col. 3: 25-30 "... CAS...").

Per claim 19, Dice discloses the method of claim 1, embodied in operation of an application programming interface (API) that includes a load operation and an multi-target compare and swap (NCAS) operation (col. 3: 25-30 "... CAS..." and e.g. FIG. 5, 404 and related text).

Per claim 20, Dice discloses the method of claim 19, wherein the load operation is wait-free (col. 6: 20-40 "... ownership of the critical code ... first user process interruption ...").

Per claim 21, Dice discloses the method of claim 1, embodied in operation of an application programming interface (API) that provides transactional memory (e.g. FIG. 5, 404 and related text).

Per claim 22, Dice discloses an implementation of non-blocking, multi-target transactions that employs instances of one or more single-target synchronization primitives to acquire, for a particular multi-target transaction, ownership of targeted transactionable locations and to ensure that, at commit (col. 21: 15-25 "... memory information committed such as writing the contents of registers out ...").

Dice does not explicitly discloses the particular multi-target transaction continues to own each of the targeted transactionable locations, wherein individual ones of the multi-target transactions do not contribute to progress of another. However, Newell discloses blocking or committing will occur when a task attempts to access a memory location which is owned by another task (e.g. FIG. 8 and 9). If the blocked task is allowed to continue, then a state transition

back to ACTIVE (bubble 204) for that task occurs, and the blocking task undergoes a state transition from ACTIVE (bubble 204) to ROLLBACK (bubble 208) of FIG. 8 (col. 9:20-35). Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to combine Dice and Newell to continue the ownership locations by disallowing state transition for the blocked task in the ACTIVE state as once suggested by Newell col. 9:20-35).

Per claim 23, Dice discloses the implementation of claim 22, embodied as software encoded in one or more computer readable media and that, on execution as part of a concurrent computation, invokes the multi-target transactions (col. 7: 1-10 "... code that is to be invoked upon returning ...").

Per claim 24, Dice discloses the implementation of claim 22, wherein the ownership acquiring, when performed by a first one of the multitarget transactions, wrests ownership from respective other ones of the multi-target transactions, if any, that own respective ones of the targeted transactionable locations (col. 6: 20-40 "... ownership of the critical code ... first user process interruption ...").

Per claim 25, Dice discloses the implementation of claim 24, wherein the wresting employs an instance of single-target synchronization primitive to change status of a wrested-from transaction to be incompatible with a commit thereof (col. 21: 1-15 "... change during interruption ...").

Per claim 26, Dice discloses the implementation of claim 25, wherein, as a result of the status change, the wrested-from transaction eventually fails and retries (col. 3:15-30 "... CAS instruction at the end ... attempts to successfully execute ... each time this instruction fail ...").

Per claim 27, Dice discloses the implementation of claim 22, wherein no transaction may prevent another from wresting therefrom ownership of transactionable locations targeted by the active transaction (col. 16: 55-67 "... information can include register values ...").

Per claim 28, Dice discloses the implementation of claim 22, wherein the transactionable locations directly encode the respective values (col. 16: 55-67 "... information can include register values ...").

Per claim 29, Dice discloses the implementation of claim 22, wherein the transactionable locations are indirectly referenced (col. 16: 55-67 "... information can include register values ...").

Per claim 30, Dice discloses the implementation of claim 22, wherein the transactionable locations are encoded in storage managed using a nonblocking memory management technique (col. 10: 10-20 "... technique lock-free ...").

Per claim 31, Dice discloses the implementation of claim 22, wherein the transactionable locations, if unowned, directly encode the respective values and otherwise encode a reference to the owning transaction (col. 6: 45-50 "... inability to obtain ownership ...").

Per claim 32, Dice discloses the implementation of claim 22, wherein at least some instances of the single-target synchronization primitive employ a Compare-And-Swap (CAS) operation.

Per claim 33, Dice discloses the implementation of claim 22, wherein at least some instances of the single-target synchronization primitive employ a Load-Linked (LL) and Store-Conditional (SC) operation pair.

Per claim 34, Dice discloses the implementation of claim 22, wherein at least some of the multi-target transaction have semantics of a multitarget compare and swap (NCAS) operation.

Per claim 35, Dice discloses the implementation of claim 22, embodied as software that includes a functional encoding of operations concurrently executable by one or more processors

to operate on state of the transactionable locations (col. 16: 55-67 "... information can include register values ...").

Per claim 36, Dice discloses the implementation of claim 22, wherein at least some of the multi-target transactions are defined by an application programming interface (API) that includes a load operation and a multi-target compare and swap (NCAS) operation.

Per claim 37, Dice discloses the implementation of claim 22, wherein at least some of the multi-target transactions are defined by an application programming interface (API) that provides transactional memory.

Per claim 38, Dice discloses the implementation of claim 22, wherein the multi-target transactions are obstruction-free, though not wait-free or lock-free.

Per claim 39, Dice discloses the implementation of claim 22, wherein the implementation does not itself guarantee that at least one interfering concurrently executed multi-target transactions makes progress (col. 7: 1-10 "... code that is to be invoked upon returning ...").

Per claim 40, Dice discloses the implementation of claim 22, wherein a contention management facility is employed to facilitate progress in a concurrent computation (col. 7: 1-10 "... code that is to be invoked upon returning ...").

Per claim 41, Dice discloses the implementation of claim 40, wherein operation of the contention management facility ensures progress of the concurrent computation (col. 21: 15-25 "... memory information committed such as writing the contents of registers out ...").

Per claim 42, Dice discloses the implementation of claim 40, wherein the contention management facility is modular such that alternative contention management strategies may be employed without affecting correctness of the implementation (col. 21: 15-25 "... memory information committed such as writing the contents of registers out ...").

Per claim 43, Dice discloses the implementation of claim 40, wherein the contention management facility allows changes in contention management strategy during a course of the concurrent computation (col. 9: 1-20 "... allow to reverse change ...").

Per claim 44, this is the program product version of the claimed method discussed above (Claim 22), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 45, this is the program product version of the claimed method discussed above (Claim 24), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 47, this is the computer readable medium version of the claimed method discussed above (Claim 7), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 48, this is the computer readable medium version of the claimed method discussed above (Claim 4), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 49, this is the computer readable medium version of the claimed method discussed above (Claim 15), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 50, this is the computer readable medium version of the claimed method discussed above (Claim 16), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 51, this is the computer readable medium version of the claimed method discussed above (Claim 17), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 52, this is the computer readable medium version of the claimed method discussed above (Claim 1), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 53, this is the computer readable medium version of the claimed method discussed above (Claim 18), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 54, this is the computer readable medium version of the claimed method discussed above (Claim 5), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 55, Dice discloses a encoding of claim 46, wherein the computer readable medium includes at least one medium selected from the set of a disk, tape or other magnetic, optical, or electronic storage medium and a network, wireline, wireless or other communications medium (e.g. FIG. 1, 120 and related text).

Per claim 56, this is the apparatus version of the claimed method discussed above (Claim 1), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 57, this is the computer readable medium version of the claimed method discussed above (Claim 7), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 58, this is the computer readable medium version of the claimed method discussed above (Claim 2), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Per claim 59, this is the computer readable medium version of the claimed method discussed above (Claim 4), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Dice.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TUAN DAM
SUPERVISORY PATENT EXAMINER

Isaac Tecklu
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